DSP II Final Project Template

Email one **pdf** file (*not msword*), and turn in **3** hardcopies per group of 2 students, 1 hardcopy kept by instructor.

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*Abstract*—This report summarizes whatever. In this project, the mbed.org interface was used to compile a FRDM-K64F project that caused LED\_2 (red LED) to flash on and off approximately twice per second, and caused the digital-to-analog converter (DAC) to implement negative capacitance. Results included are: 1) software code, 2) measured clock frequencies and capacitance, and 3) oscilloscope waveforms. Blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah.

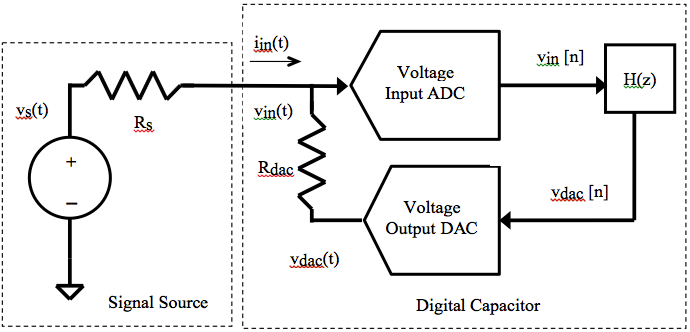


Fig. 1. Block diagram of digital negative capacitor.

# Introduction

***Project reports must be exactly 3 pages long and in this format, with approximaely same proportions of space allocated to the figures, and each section.***.

Non-Foster circuit elements such as negative capacitors and negative inductors offer the potential for significant performance improvement in metamaterials, antennas, …blah, blah, blah [1-2]. These non-Foster have historically been constructed using Linvill circuits and current conveyors [3-4]. However, stability is often a concern in such analog circuit approaches [5]. Therefore, we consider a new digital design approach offering greater control of performance and stability.

In this project, we investigate a digital negative capacitor blah, blah, blah, blah, blah, blah, blah, blah, blah, blah. Earlier Weldon describes the fundamentals of a digital negative capacitor, where ….blah, blah, blah, blah, blah [6]. In a second article, Weldon describes stability analysis….blah, blah, blah, blah, blah [7]. Blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah.

In the following, Blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah

# Theory

The block diagram of the proposed digital negative capacitor is shown in Fig. 1, along with a driving voltage source with source resistance Rs. The input voltage vin(t) is digitized by the ADC (analog-to-digital converter) to form vin[n]. Then, vdac[n] = vin[n]\*h[n], with z-tranform Vdac(z)=Vin(z)H(z). The DAC (digital-to-analog converter) converts vdac[n] into continuous-time voltage vdac(t), and then iin(t)=vin(t)-vdac(t))/Rdac . Based on the theory provided in [2] and [3], where the DAC current *i(t)* is

**** 

where *v[n]* is the analog-to-digital converter ADC sampled voltage, *C* is the capacitance, and *T* is the ADC and DAC sampling period.

Blah, blah, ….

Blah, blah, ….

 

where R is… blah, blah, blah, blah, blah

Blah, blah, ….

Blah, blah, ….

 

where R is… blah, blah, blah, blah, blah

blah, blah, blah, blah, blah Blah, blah, ….

Blah, blah, ….

 

where R is… blah, blah, blah, blah, blah

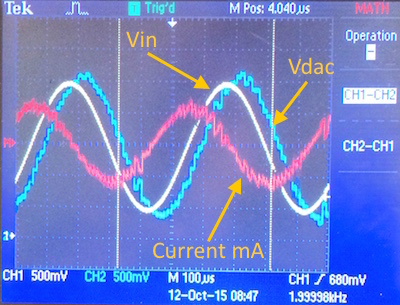


Fig. 3. Fix me Measured data for 40 nF positive capacitor, with xx KHz sine wave input. Blue trace is ADC input voltage, red trace blah, blah, blah ***Do not use photographs as shown here****, load proper traces from the oscilloscope onto a USB stick with white backgrounds for ALL oscilloscope traces*

Ticker timer1;

….

timer1.attach(&myDsp,12.5e-6f);

…

y=-2.2f\*x+3.2f\*xold;

//y=-1.2f\*x+7.7f\*xold

Fig. 2. Fix me Code excerpt to implement positive (40 nF) and negative (-40 nF) capacitor, with negative capacitor line commented out.

Blah, blah, ….

 

where R is… blah, blah, blah, blah, blah. blah, blah, stable if poles are inside unit circle, so blah, blah,

Fix this line T/(RsC)<-xxx ***or*** T/(RsC)>>xx 6

Blah, blah, ….

# Implementation And Software Code

*For your software, do not include the entirety of your code, rather, include only the most important lines of code for a task.*

The negative capacitor of Fig. 1 was implemented on a Freescale FRDM-K64F board, using an mbed compiler[8-9]. The software to implement the negative capacitance is provided in the software code excerpt of Fig. 2. An xx us timer interruot was used to blah, blah… Inside the myDsp() interrupt service routing, a positive 40 nF blah blah is implemented by y=0.2x+0.3y blah, blah… The commented line …blah blah …a -40 nF blah blah y=0.2x+0.3y … blah blah blah blah …The stability factor of the positive cap, blah, …The stability factor of the -40 nF cap

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# Measured Data

*For your measured data, include only the most important data and oscilloscope plots, and/or any specific items required by the project description*. The software was loaded onto the FRDM-K64F board after compiling …mbed and blah, blah. As part of the experiment, K64F blah, blah,blah and capacitance were also measured and are given in Table I below.

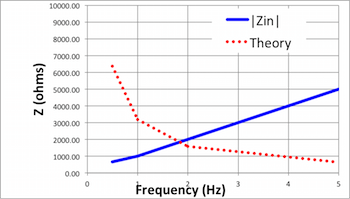


Fig. 4. Fix me Measured data for positive capacitor. Blue trace is blah red trace is blah, blah, blah, blah is blah, blah, blah, blah is blah, blah, blah, blah is blah, blah, blah, blah.***Do not use illegible fonts as shown here!***

1. Measured Data Summary

| Parameter | Expected | Measured |
| --- | --- | --- |
| Fix me | 120 MHz | 100 MHz |
| Fix | 60 MHz | 25 MHz |
| Measured Capacitance | -10 nF | -8.8 nF |

The system core clock was … Blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah …The stability factor of the positive cap, blah, …The stability factor of the -40 nF cap, blah,blah, blah, blah. Blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah.

Fig. 3 shows waveforms (*Do not use photographs as shown here, load proper traces from the oscilloasope onto a USB stick with white backgrounds for ALL oscilloscope traces*) at the ADC (yellow) and DAC (blue) were measured using a Tek2001a oscilloscope, using a xx KHz sine wave. The 8.8 nF measured capacitance in Table I is based on blah, blah voltage waveform and current waveform in Fig. 3. Blah, blah, blah

Fix me The measured magnitude of Z(s) from (4) is plotted Fig. 4 for sinusoidal input from x to y KHz. Theoretical y=0.2x+0.3y is shown in dashed red blah, blah, blah measure blah, blah, blah in solid blue blah, blah, blah , As can be seen, blah, blah, blah

Blah

Fix me Fig. 5 shows waveforms (*Do not use photographs as shown here, load proper traces from the oscilloscope onto a USB stick with white backgrounds for ALL oscilloscope traces*) at for a xx KHz triangle wave input at the ADC (yellow) and DAC (blue) were measured. The blue trace is ADC input voltage, the red trace blah, blah, blah. The peak current blah, blah MATH mode blah, blah voltage waveform and current waveform in Fig. 5. Blah, blah, bla The 8.8 nF measured capacitance in Table I is based on blah, blah voltage waveform and current waveform. … Blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah. Blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah Blah, blah, blah xx

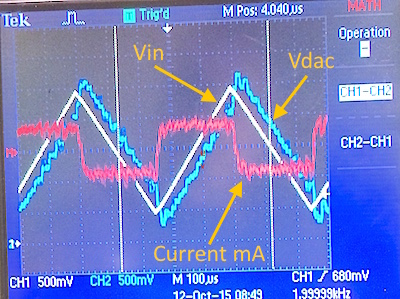


Fig. 5. Fix me Measured data for 40 pF positive capacitor, using xx KHz triangle wave input. Top blue trace is voltage, bottom red trace is current. ***Do not use photographs as shown here****, load proper traces from the oscilloscope onto a USB stick with white backgrounds for ALL oscilloscope traces*

Fix me Fig. 6 shows waveforms (*Do not use photographs as shown here, load proper traces from the oscilloasope onto a USB stick with white backgrounds for ALL oscilloscope traces*) at for a xx KHz triangle wave input at the ADC (yellow) and DAC (blue) were measured. The blue trace is ADC input voltage, the red trace blah, blah, blah. The peak current blah, blah MATH mode blah, blah voltage waveform and current waveform in Fig. 6. Blah, blah, bla The 8.8 nF measured capacitance in Table I is based on blah, blah voltage waveform and current waveform. … Blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah. Blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah blah, blah yy

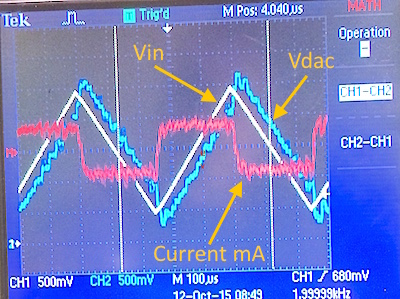


Fig. 6. Fix me Measured data for -40 pF capacitor, using xx KHz triangle wave input.. Top blue trace is voltage, bottom red trace is current. ***Do not use photographs as shown here****, load proper traces from the oscilloscope onto a USB stick with white backgrounds for ALL oscilloscope traces*

… Blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah. Blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah, blah

blah, ….

# Summary

Prototype of new digital discrete-time positive and negative capacitors were built using the Freedom-K64F blah, blah. The 40 nF positive digital capacitor was measured to have xx nF using a trinagle wave ecitation at xx KHz. The -40 nF digital capacitor was measured to have -xx nF using a trinagle wave ecitation at xx KHz. The frequency response of the positive capacitor blah, blah, matched theory, blah blah, as expected.

##### References (*5 references minumum are required*)

*At least 1 reference must be an IEEE paper*

1. Find this refernce. Hint: read my papers on my website.
2. And find this one. Hint: read my papers.
3. Linvill, find it. Hint: read my papers.
4. Sedra, find it. Hint: read my papers.
5. Stearns, find it. Hint: read my papers.
6. T.P. Weldon, J.M.C. Covington III, K.L. Smith, and R.S. Adams ``Performance of Digital Discrete-Time Implementations of Non-Foster Circuit Elements,'' *2015 IEEE Int. Sym. on Circuits and Systems*, Lisbon, Portugal, May 24-27, 2015.
7. T.P. Weldon, J.M.C. Covington III, K.L. Smith, and R.S. Adams, ``Stability Conditions for a Digital Discrete-Time Non-Foster Circuit Element,'' *2015 IEEE Int. Symposium on Antennas and Propagation*, Vancouver, BC, Canada, July 19-25, 2015.
8. *FRDM-K64F Freedom Module User’s Guide*. [Online]. Available: http://cache.freescale.com/files/32bit/doc/user\_guide/FRDMK64FUG.pdfh
9. Mbed find it