Embedded Sig. Proc. Project 99: DAC/Blinky

Email one **pdf** file (*not msword*), and turn in **3** hardcopies per group of 2 students, , 1 hardcopy kept by instructor.

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*Abstract*—This report summarizes Project 0: DAC/Blinky. In this project, the mbed.org interface was used to compile a FRDM-K64F project that caused LED\_2 (red LED) to flash on and off approximately twice per second, and caused the digital-to-analog converter (DAC) to implement negative capacitance. Results included are: 1) software code, 2) measured clock frequencies and capacitance, and 3) oscilloscope waveforms.

# Introduction

***Project reports may not exceed one page.*** The FRDM-K64F board includes a 10-bit digital-to-analog converter (DAC) and a red light-emitting diode [1]. The board is to be programmed to 1) blink the red LED on and off approximately at a rate of 2.5 Hz, 2) set the system core clock to 120 MHz, 3) set the bus clock to 60 MHz, and 4) implement a capacitance of 10 nF at the DAC output. The following sections present the theory, software code, and measured data.

# Theory

The negative capacitance is based on the theory provided in [2] and [3], where the DAC current *i(t)* is

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where *v[n]* is the analog-to-digital converter ADC sampled voltage, *C* is the capacitance, and *T* is the ADC and DAC sampling period.

# Software Code

*For your software, do not include the entirety of your code, rather, include only the most important lines of code for a task.*  The software to implement the blinking LED is provided in the software code excerptof Fig. 1 below.

 DigitalOut led\_green(LED\_GREEN);

…

 led\_green = 0;

 wait(0.5f);

 led\_green = 1;

Fig. 1. Code excerpt to implement flashing LED.

The software to implement the negative capacitance of (1) is implemented in the software excerpt of Fig. 2 below:

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 int cap= 10, period=0.001,current=0;

…

 current = (uint32\_t) (cap/period)\*(vin – vin\_old);

Fig. 2. Code excerpt to implement current i(t).

# Measured Data

*For your measured data, include only the most important data and oscilloscope plots, and/or any specific items required by the project description*. The software was loaded onto the FRDM-K64F board and the red LED bliked at 2.5 Hz, as expected. As part of the experiment, K64F clock frequencies and capacitance were also measured and are given in Table I below.

1. Measured Data Summary

| Parameter | Expected | Measured  |
| --- | --- | --- |
| System Core Clock | 120 MHz | 100 MHz |
| Bus clock | 60 MHz | 25 MHz |
| Measured Capacitance | -10 nF | -8.8 nF |

In addition, the waveforms at the DAC were measured using a Tek2001a oscilloscope, using a 200 MHz triangle wave, and shown in Fig. 3 below. The -8.8 nF measured capacitance in Table I is based on i=C*dv/dt* for the voltage waveform and current waveform in Fig. 3.

 

 (a) (b)

Fig. 3. (a) Measured data for negative capacitor. Top blue trace is voltage, bottom red trace is current. (b) FRDM-K64F prototype with test probes.

##### References (*Two references minumum are required*)

*At least 1 reference must be an IEEE paper*

1. *FRDM-K64F Freedom Module User’s Guide*. [Online]. Available: http://cache.freescale.com/files/32bit/doc/user\_guide/FRDMK64FUG.pdfh
2. T.P. Weldon, J.M.C. Covington III, K.L. Smith, and R.S. Adams ``Performance of Digital Discrete-Time Implementations of Non-Foster Circuit Elements,'' *2015 IEEE Int. Sym. on Circuits and Systems*, Lisbon, Portugal, May 24-27, 2015.
3. T.P. Weldon, J.M.C. Covington III, K.L. Smith, and R.S. Adams, ``Stability Conditions for a Digital Discrete-Time Non-Foster Circuit Element,'' *2015 IEEE Int. Symposium on Antennas and Propagation*, Vancouver, BC, Canada, July 19-25, 2015.