A Prototype Single-Chip Spectrum Analyzer with Integrated Frequency-Synthesized Tuning

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***Abstract* — A variety of applications such as spectrum monitoring systems and dynamic spectrum access systems motivate the development of on-chip capability to measure the frequency spectrum of the local radio environment. Toward this end, a prototype of a simple single-chip frequency-synthesized spectrum analyzer is presented. The design is targeted for applications where the spectrum analyzer would be a component of a larger complex system. Therefore, a simple architecture is considered in order to minimize chip area and reduce power consumption. Although the proposed spectrum analyzer architecture is uncomplicated, it nevertheless provides useful baseline capability for measurement of the frequency spectrum. A prototype was fabricated in a standard 0.5 micron CMOS process, and measured results are given from 20 to 200 MHz.**

I. INTRODUCTION

The explosive growth of wireless devices and applications, combined with the scarcity of available frequency spectrum, has motivated considerable research into efficient utilization of available spectrum. As a consequence, there is increasing need for a variety of spectral monitoring systems and dynamic spectrum access systems [1]-[5]. In contrast with conventional fixed spectrum allocation, dynamic spectrum access methods offer the potential for more efficient use of underutilized spectrum such as television bands [4]. One common thread in these systems is the need to characterize the local frequency spectrum, and this motivates the present investigation of a simple on-chip spectrum analyzer. Although a variety of other approaches such as cognitive radio systems and software defined radio systems can be used to implement dynamic spectrum access, the proposed spectrum analyzer is amenable to a variety of applications [1].

In order to reduce chip area and power consumption, a simple system architecture is chosen for the proposed single-chip spectrum analyzer. The proposed design is distinct from prior spectrum analyzer approaches for other applications. Among these approaches, monolithic switched capacitor implementations have limited bandwidth [7], and signal processing approaches require high speed analog-to-digital converters, fast memory, and Fast Fourier Transform (FFT) hardware or off-line FFT processing [8]. Other approaches, such as surface-acoustic-wave devices, cannot be readily implemented in a standard CMOS process [9].

The foregoing limitations in these prior systems motivate the development of the proposed on-chip frequency-synthesized spectrum analyzer. In this, a simple ac-coupled zero intermediate frequency (zero-IF) system with logarithmic video output is proposed. Also, a frequency synthesizer is included to provide frequency accuracy. Although a more complicated architecture could provide improved performance, the present design focuses on a minimum-complexity architecture to conserve chip area and to reduce power consumption. In addition, measured experimental results for the proposed system offer useful baseline performance data and provide insight into fundamental capabilities of elementary spectrum analyzer architectures. Furthermore, the proposed design may provide sufficient performance for various applications, and the measured data is useful in evaluating such design considerations.

In the following sections, the design of the proposed spectrum analyzer is first described, including the frequency synthesizer section. Then, measured data up to 200 MHz is presented for a prototype integrated circuit using a 0.5 micron CMOS process.

II. SPECTRUM ANALYZER DESIGN

To meet the design objective of minimizing complexity, an ac-coupled zero-IF architecture was selected for the proposed spectrum analyzer integrated circuit. The zero-IF method eliminates the need for image rejection filters, IF filters, and associated circuitry. The use of ac coupling eliminates dc-offset problems at the cost of a small deadband near center frequency. This deadband can be mitigated by adjusting the frequency sweep, by dithering the local oscillator frequency, or by inherent broadband characteristics of target signals. Finally, a basic frequency synthesizer is included in the design to provide frequency accuracy in the overall spectrum analyzer.

A block diagram of the proposed single-chip spectrum analyzer is shown in Fig. 1, where the Frequency Synthesizer

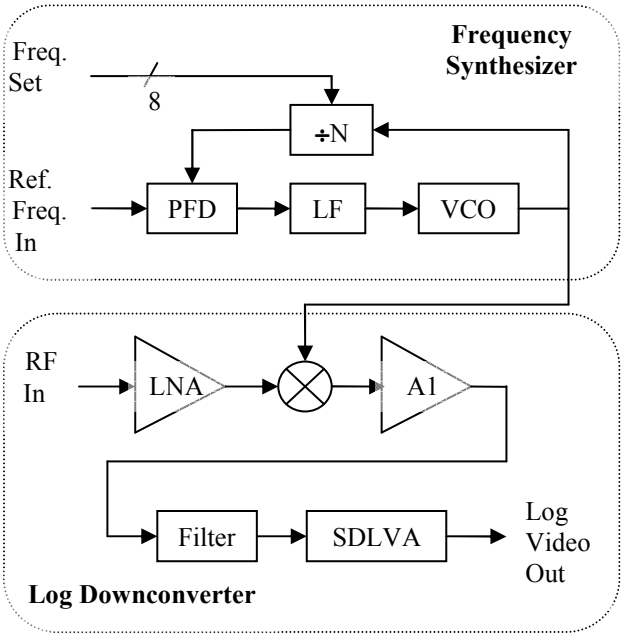

Figure 1. Block diagram of the proposed single chip Spectrum Analyzer with frequency synthesized tuning. Spectrum Analyzer and Frequency Synthesizer blocks are marked for clarity.

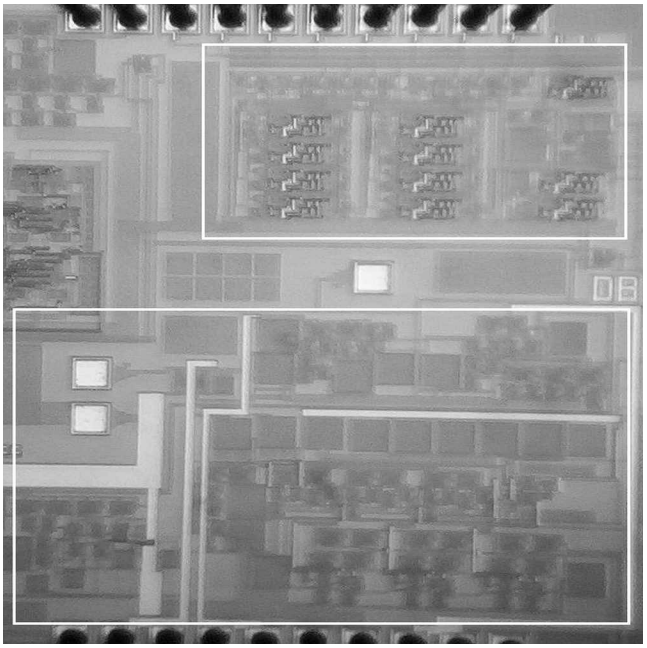

Figure 2. Photograph of single-chip spectrum analyzer; upper box surrounds frequency synthesizer, lower box surrounds remainder of spectrum analyzer.

and Log Downconverter sections of the overall spectrum analyzer are outlined in dashed blocks.

In the upper left corner of the Frequency Synthesizer section, an 8-bit wide parallel input bus (Freq. Set) sets the frequency divider ratio, N. The output of the frequency divider and the reference frequency signal (Ref. Freq. In) are fed to the phase frequency detector (PFD). The output of the PFD drives the loop filter (LF), which in turn drives the voltage-controlled oscillator (VCO). The output of the VCO is then fed back to the frequency divider and is also applied to local oscillator port of the mixer in the Log Downconverter section.

In the Log Downconverter section at the bottom of Fig. 1, the radio frequency input (RF In), is first amplified to a low noise amplifier (LNA). The amplified RF signal is then applied as input to the mixer along with the VCO output of the frequency synthesizer. The output of the mixer is amplified in an ac-coupled amplifier (A1), and is then low-pass filtered. Finally, the low-pass filtered signal is fed to a successive-detection log video amplifier (SDLVA). The SDLVA produces an output voltage that is logarithmically proportional to the signal strength and forms the final output of the spectrum analyzer [11].

The foregoing design was implemented in a standard 0.5 micron CMOS process, and a photograph of the fabricated prototype is shown in Fig. 2. The white box in the upper right of the figure encloses the frequency synthesizer and is approximately 800×400 microns in size. The white box in the lower half of Fig. 2 encloses the remainder of the spectrum analyzer and is approximately 1200×800 microns in size.

III. RESULTS

The fabricated frequency-synthesized spectrum analyzer chip of Fig. 2 was first tested with an RF input signal of -10 dBm at 100MHz, while the log video output was measured as shown in Fig. 3.

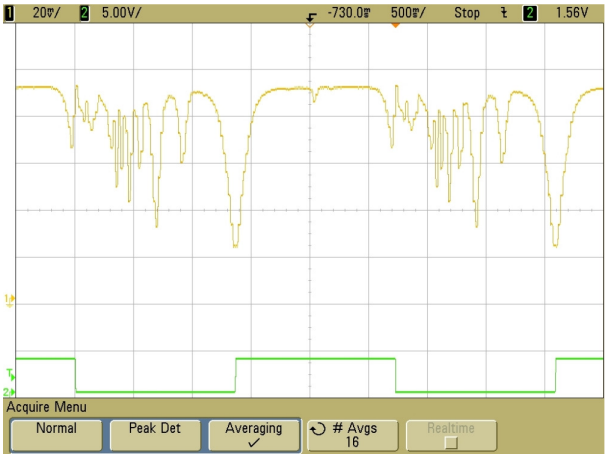

Figure 3. Spectrum analyzer: measured spectrum of a -10 dBm 100 MHz sinusoid. Horizontal axis is RF input frequency. Upper trace vertical axis is logarithmic video output voltage, at 20 mV/div. Bottom trace: falling edge indicates frequency synthesizer transition from 200 MHz to 1.56 MHz, rising edge indicates 100 MHz. Large dip in upper trace indicates strong 100 MHz RF input signal. Output is inverted, where lower voltages indicate stronger signals.

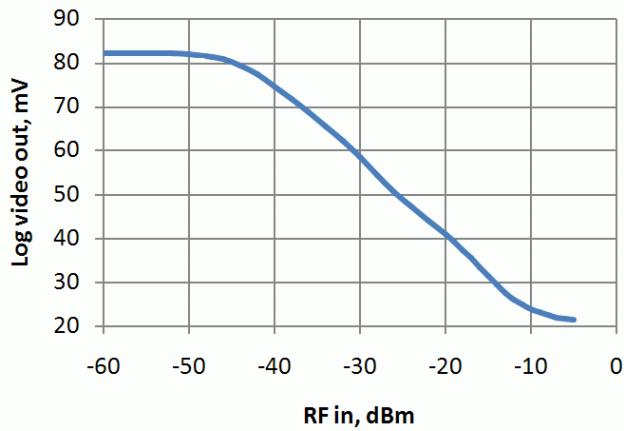

Figure 4. Spectrum Analyzer response to a 100 MHz RF input signal Horizontal axis is RF input power; vertical axis is logarithmic video output.

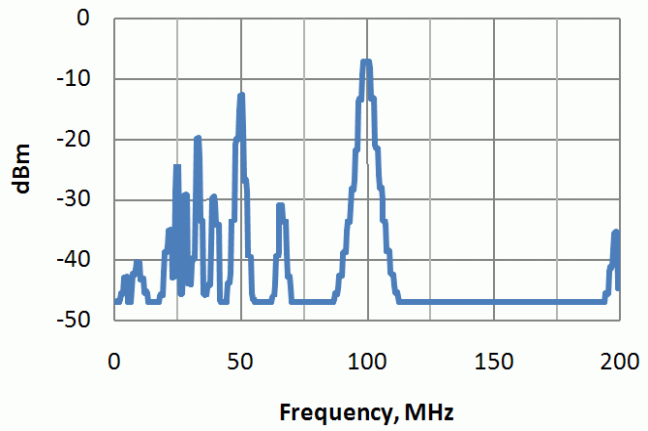

Figure 5. Spectrum analyzer: measured spectrum of a -10 dBm 100 MHz sinusoid. Horizontal axis is RF input frequency, vertical axis is logarithmic video output converted to equivalent RF power in dBm.

The upper oscilloscope trace in Fig. 3 is the logarithmic video output voltage of the spectrum analyzer chip as the frequency synthesizer varies from 1.56 MHz to 200 MHz in 128 steps. The lower trace of Fig. 3 shows the most significant bit of the Freq. Set input bus of Fig. 1. The falling edge of the lower trace is where the frequency synthesizer makes the transition from 200 MHz to 1.56 MHz, and at the rising edge of the lower trace is where the frequency synthesizer is set to 100 MHz. At the point of the rising edge in the lower trace, the spectral peak corresponding to the 100 MHz signal is seen in the upper trace where the voltage dips down to 22 mV. Note that the upper trace in Fig. 3 is an inverted version of the spectrum in Fig. 3, because the logarithmic video output is inverted for the particular SDLVA design that was used. Therefore, lower voltages in the upper trace of Fig. 3 indicate stronger signals.

To convert the logarithmic output voltages back into equivalent RF input power, the logarithmic response of the spectrum analyzer was calibrated using an RF input signal at 100 MHz. The measured relationship between RF input power and logarithmic output voltage is shown in Fig. 4. An RF signal level of -5 dBm corresponds to an SDLVA output of approx. 20 mV, and an RF signal level of -45 dBm corresponds to an SDLVA output of approx. 82 mV.

Using the logarithmic calibration curve of Fig. 4, the plot of Fig. 3 was converted into the RF spectrum of Fig. 5. In the measured frequency spectrum of Fig. 5, the 100 MHz signal is clearly visible in the middle of the spectrum. A second harmonic response is also visible at 200MHz with nearly 30 dB less power, and is caused by the LO - 2RF mixer spurious response. Other sub-harmonic responses below 100 MHz in Fig. 5 are also due to various spurious responses of the mixer. For example, the response at 50 MHz corresponds to the 2LO - RF spur, and the response at 66.7 MHz corresponds to the 3LO – 2RF spur. In practice, these spurious responses may not be of concern if pre-filtering is present, or if an antenna limits bandwidth, or if the frequency synthesizer is limited to certain smaller tuning ranges.

Test results for a -10 dBm 20 MHz RF input test signal are shown in the oscilloscope traces of Fig. 6. As before, the upper oscilloscope trace is the log video output of the spectrum analyzer, with lower voltages indicating stronger signals. Again, in the lower trace of Fig. 6 the falling edge indicates the 200 MHz to 1.56 MHz transition, and the rising edge indicates 100 MHz. The corresponding spectrum from the digitized data is shown in Fig. 7, using the logarithmic calibration curve of Fig. 4. In Fig. 7, the 20 MHz RF signal is the largest component of the spectrum. Mixer spurious responses are also visible in the spectrum of Fig. 7, similar to those noted for the 100 MHz signal of Fig. 5.

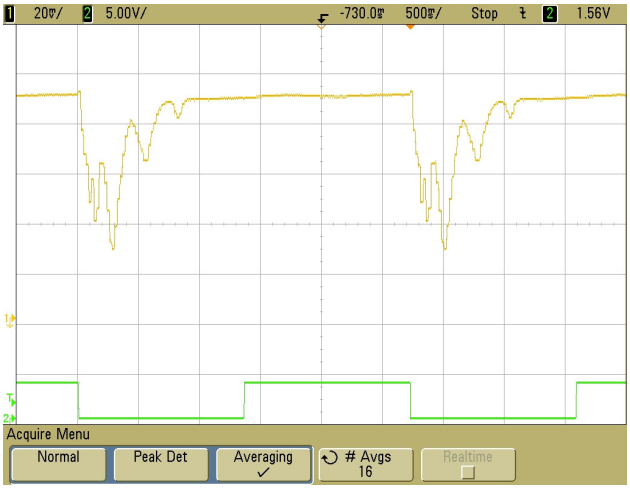

Figure 6. Spectrum analyzer: measured spectrum of a 20 MHz, -10 dBm sinusoid. Horizontal axis is RF input frequency. Upper trace vertical axis is logarithmic video output voltage, at 20 mV/div. Bottom trace: falling edge indicates frequency synthesizer transition from 200 MHz to 1.56 MHz, rising edge indicates 100 MHz. Large dip in upper trace indicates strong 20 MHz RF input signal. Output is inverted, where lower voltages indicate stronger signals.

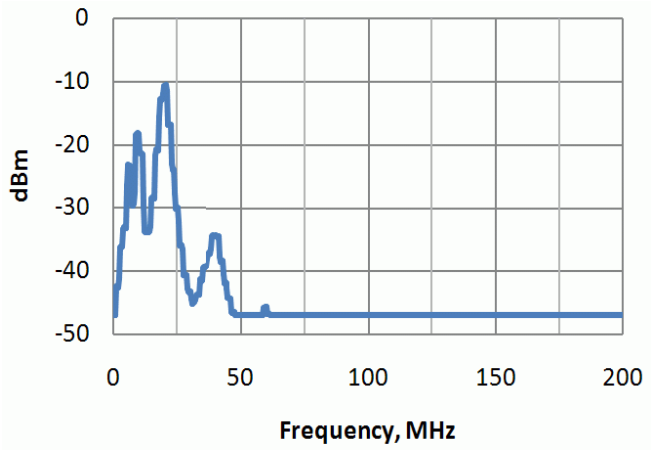

Figure 7. Spectrum analyzer: measured spectrum of 20 MHz -10 dBm sinusoid. Horizontal axis is RF input frequency, vertical axis is logarithmic video output converted to equivalent power level in dBm.

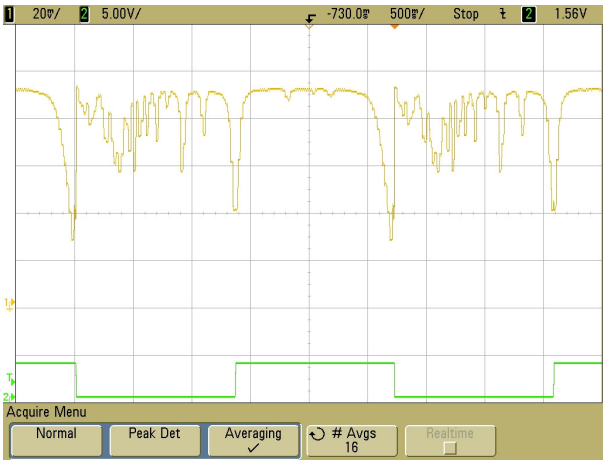

Figure 8. Spectrum analyzer: measured spectrum of a 200 MHz, -10 dBm sinusoid. Horizontal axis is RF input frequency. Upper trace vertical axis is logarithmic video output voltage, at 20 mV/div. Bottom trace: falling edge indicates frequency synthesizer transition from 200 MHz to 0 Hz, rising edge indicates 100 MHz. Large dip in upper trace indicates strong 200 MHz RF input signal. Output is inverted, since lower voltages indicate stronger signals.

Finally, test data is given in Fig. 8 and Fig. 9 for a -10 dBm 200 MHZ sinusoidal RF input test signal. The 200 MHz signal is evident as the dip in the upper trace of Fig. 8, directly above the high-to-low transition of the lower trace. The corresponding spectrum from the digitized data is shown in Fig. 9, using the logarithmic calibration curve of Fig. 4. In Fig. 9, the 200 MHz signal is at the far right. The response at 100 MHz corresponds to the 2LO - RF spur.

IV. Conclusion

A prototype 200 MHz frequency-synthesized single-chip spectrum analyzer has been fabricated in 0.5 micron CMOS. Test results demonstrate operation from 20 MHz to 200 MHz. The prototype integrated circuit demonstrates baseline capabilities of the proposed simple spectrum analyzer architecture.

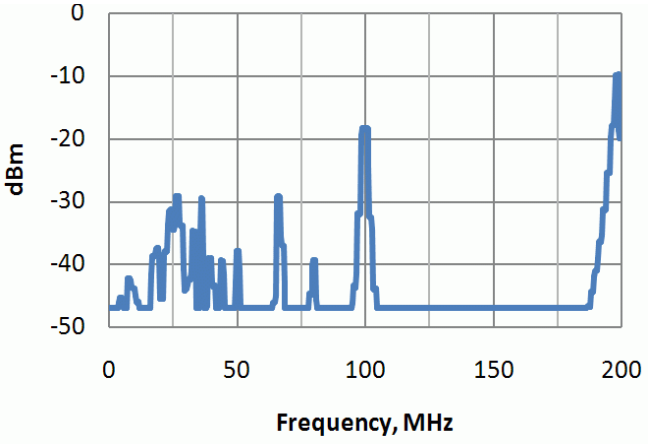

Fig. 9 Spectrum analyzer: measured spectrum of 200 MHz -10 dBm sinusoid. Horizontal axis is RF input frequency, vertical axis is logarithmic video output converted to equivalent power level in dBm.

Acknowledgement

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